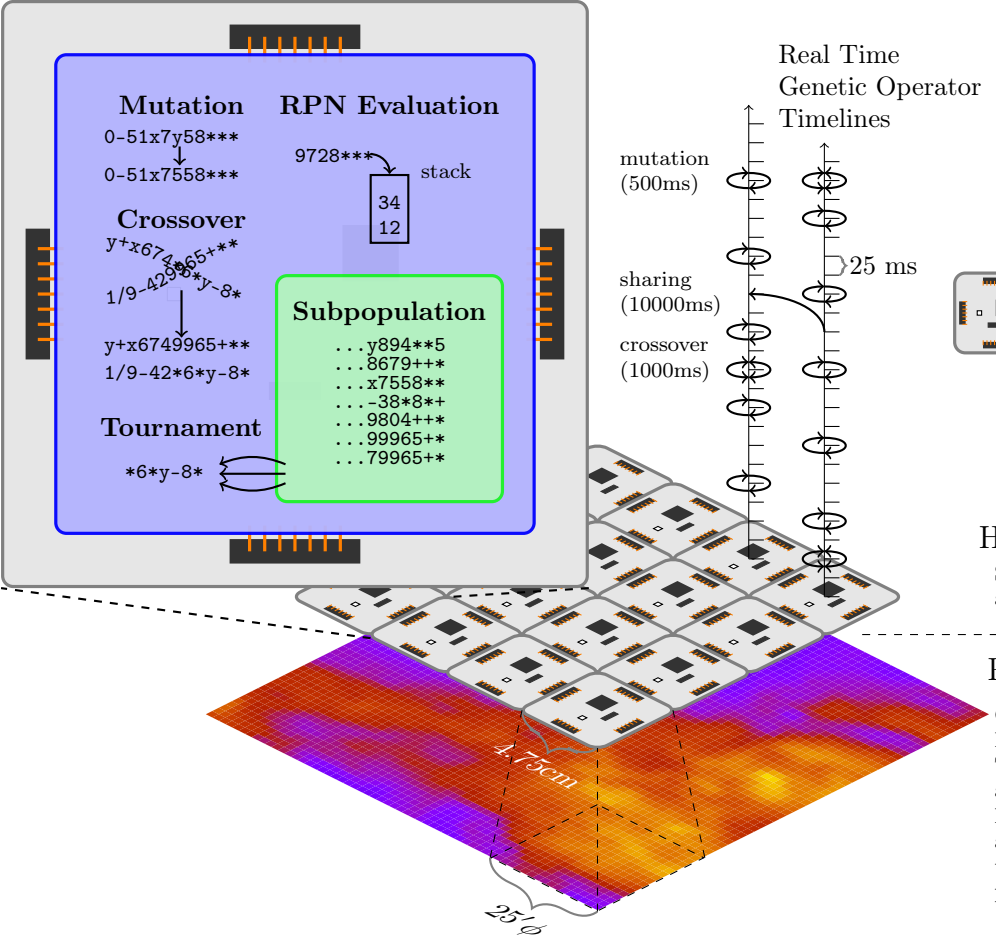

Each tile includes

- 32-bit ARM processor
- 32KB RAM
- 16KB EEPROM
- 512KB Flash
- 128KB problem data storage
- hardware timers
- intertile power sharing
- 4 serial ports

Hardware Space

Sixteen $4.75cm \times 4.75cm$ tiles arranged in a 4×4 square.

Problem Space

Gravity data from the state of Montana. Each hardware tile covers $25'\phi \times 25'\lambda$. The size and shape of the total covered area is determined by the number and layout (Section 4.3) of the hardware tiles, and by the scale and scheme (Section 4.2) used to map the hardware space to the problem space.